IN THE SPECIFICATION

Please replace the paragraph beginning at line 2, page 7 with the following rewritten paragraph:

Figure 1 illustrates an embodiment of a semiconductor on insulator (SOI) semiconductor device 100 in accordance with the present invention. SOI device 100 may reside on bulk silicon 101 referred to as the "substrate." SOI device 100 may further comprise a layer of oxide 102, referred to as the "box insulator," residing on the bulk silicon 101. In one embodiment, oxide 102 may be composed of SiO_2. On top of box insulator 102 may reside a silicon region, referred to as the "body" 103. Body 103 may include active regions ~~104A-B~~ 104A-104B, e.g., source/drain junctions, and shallow trench isolation (STI) regions ~~105A-B~~ 105A-105B. Active regions 104A-B may collectively or individually be referred to as active regions 104 or active region 104, respectively. STI regions ~~105A-B~~ 105A-105B may collectively or individually be referred to as STI regions 105 or STI region 105, respectively. Active regions ~~104A-B~~ 104A-104B may be interconnected to metal-1 layer (not shown) via contacts ~~106A-B~~ 106A-106B, respectively. Further, the top of SOI device 100 may be interconnected with a polysilicon gate 107 via contact 106C. Contacts ~~106A-C~~ 106A-106C may collectively or individually be referred to as contacts 106 or contact 106, respectively. In one embodiment, contacts 106 may be comprised of tungsten. Polysilicon gate 107 may be separated from body 103 by a gate oxide 108. Contacts 106, polysilicon gate 107 and gate oxide 108 may be interposed by an interlayer dielectric 109. It is noted that SOI device 100 may comprise any number of contacts 106, active regions 104, STI regions 105, gates 107 and gate oxide regions 108, and that Figure 1 is illustrative.

Please replace the paragraph beginning at line 9, page 8 with the following rewritten paragraph:

A method for performing passive voltage contrast on SOI device 100 to detect a breakdown in gate oxide 108 as well as to detect a contact 106 that is open is discussed below in conjunction with Figure 2. Figures ~~3A-D~~ 3A-3D, as discussed further below in conjunction with Figure 2, illustrate embodiments of SOI device 100

after the steps of etching the substrate using a dimpler, etching the substrate using tetramethylammonium hydroxide (TMAH), etching the substrate and box insulator using hydrofluoric acid (HF) are performed, and applying carbon ink are performed, respectively. Figure 4, as discussed further below in conjunction with Figure 2, illustrates an embodiment of the present invention of a passive voltage contrast chamber used for detecting a breakdown in the gate oxide of the SOI device as well as for detecting a contact 106 that is open.